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09/486,908	05/11/2000	STEFAN PFAB	P00.0365	9541

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EXAMINER
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 18

Application Number: 09/486,908
Filing Date: May 11, 2000
Appellant(s): PFAB, STEFAN

Mark Bergner
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/5/03.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-7 and 9-14 stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,787,475	Pawlowski	7-1998

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-7 and 9-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Pawlowski (US Patent # 5,787,475).

With respect to claims 1 and 9, Pawlowski discloses a data storage device (main memory and I/O module) (see column 4, lines 5-15) comprising:

memory cells having stored data with selectable output addresses (see column 4, lines 34-45, 54-60, and figure 1, item 14), wherein the specific starting address provided by a request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the requested data and outputs the requested data with cache lines, which are considered to be the selected output start address;

wherein the storage device responds to a data output request (peripheral device) by outputting the stored data beginning with a selected output start address (see column 4, lines 34-45 and column 5, line 66 to column 6, lines 10; and column 6, lines 19-35 and 50-59), wherein the specific starting address provided by the request of data is used to determine which cache line or consecutive cache lines in memory contain a beginning portion of the request data, and outputting the requested data with cache lines or consecutive cache lines, which are considered to be the selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data in response to the data output request (see column 6 lines 30-35; column 7, lines 15-25; column 9 line 56 to column 10, line 15; column 11, lines 45-58,

and column 11, line 64 to column 12, line 8). Data retrieved by the I/O controller to determine which cache line of data contains the beginning portion of address requested by the peripheral from the memory. If this beginning portion of the address is in the first cache line, then the data output to requested data by the first cache line. However, if the retriever determines that a next consecutive cache line contains the beginning portion of the requested data, the retriever increments the starting address and uses the incremented starting address to request the consecutive cache lines of data from memory. In all situations, a first cache line of consecutive cache lines, the data stored in the neighboring starting address is less than the output address since if the portion of the starting address provided by the requested data is in the first cache line, the output transfers to requested data by first cache line; and if it is greater than the first cache line, the output transfers by two consecutive cache lines.

With respect to claims 2 and 10, Pawlowski discloses a the selected output start address (beginning portion of started address for outputting the data requested by a cache line) is determined utilizing address data (peripheral device) applied to the data storage (see column 4, lines 34-45 and column 5, line 66 to column 6, line 10).

With respect to claims 3 and 11, Pawlowski discloses:

the selected output start address is determined by further utilizing adaptation data (data retriever) applied to the data storage (see column 9, lines 22-42; and column 9, line 64 to column 10 line 15);

the adaptation data (data retriever) is related both to the output start address to be employed and an address that is defined by the address data (peripheral device) (see column 6, lines 30-35).

With respect to claims 4 and 12, Pawlowski discloses:

output terminals (address and data lines) in figure 1, items 32 and 34;

an interface provided between memory cell of the data storage device and the output terminals wherein said adaptation data are used to control said interface, as shown by the I/O I/F, item 44 in figure 2.

With respect to claims 5 and 13, Pawlowski discloses the interface comprising a multiplexer that is driven based on the adaptation data, by teaching in column 6, lines 30-35, that upon receiving a data request from the peripheral over data line 32, address line 34, and command line 30, the I/O interface 44 will send the address portion of the request to the data retriever. Also, column 8, lines 5-20 teach of the combinatorial logic elements in the I/O module and interface.

With respect to claims 6 and 13, Pawlowski discloses using a prefetch system wherein the first cache line and second cache connected as a consecutive cache line for transferring the data to a requested data (peripheral device), and based on the beginning portion of the address provided by the requested data, if the starting address is greater than the first cache line, a consecutive line will be retrieved (see column 4, lines 54-60; column 5, line 66 to column 6, line 19, and column 7, lines 15-25). In other words, data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected.

With respect to claims 7 and 14, Pawlowski discloses the first output start address (beginning portion of the address provided by peripheral device for cache line output from the main memory) is an address that is represented by the address data (peripheral device) applied to the data storage device (see column 5, line 59 to column 6, line 10).

(11) Response to Argument

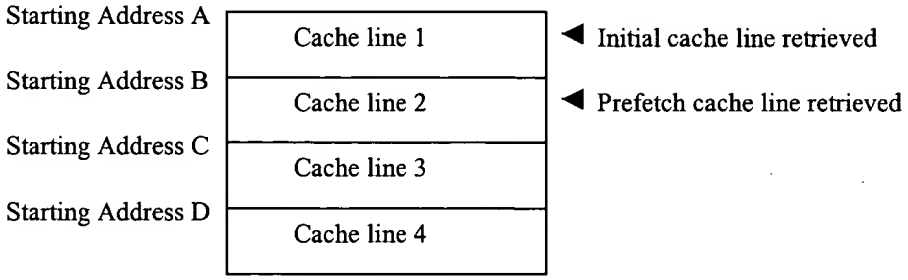
With respect to claims 1 and 9, the Applicant alleges that the data request in Pawlowski only results in the transfer of a single cache line (*i.e.*, not greater than the amount of data between neighboring start addresses). The Applicant argues that any additional prefetching of cache lines required must be made by a second request from the I/O module to the main memory.

The Applicant then argues that the claimed data storage device can only be properly equated with the main memory module 18 of Pawlowski, not the combination of the main memory module 18 and I/O module 24. The Applicant argues that this combination of elements would require extra processing which is the type of delay the present invention seeks to eliminate. However, it is noted that these features upon which applicant rely are not recited in the rejected claims. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

The Examiner believes that the overly broad term "data storage device" does not limit the scope to merely the storage medium itself, but could also incorporate other elements involved in the storage of data, especially in light of the "comprising" language in the preamble. For the purposes of this rejection, the peripheral 28 of Pawlowski issues a data request (to the main

memory module/I/O module combination), as recited in column 2, lines 30-35. This request from the peripheral will cause said main memory/I/O combination to output a plurality of cache lines back to the peripheral (the plurality of lines being the first cache line and the prefetched next consecutive cache line, as discussed in column 7, lines 10-30). The Examine believes it is reasonable to consider Pawlowski's I/O module as part of the "data storage device" because the data output request initiated by the peripheral includes a command line portion which controls the data transfer (see column 12, lines 9-25). These command line controls are essential to the data output request as they control the actual transfer of retrieved data back to the peripheral, while the system bus between the I/O module and main memory module does not include this command line portion of the full peripheral request.

As for the claim limitations regarding the amount of data that can be stored between neighboring start addresses being less than the data output in response to the request, please refer to the following illustration:



In the example above, the amount of data that can be stored between two neighboring starting addresses (for example, starting addresses A & B) would be a single cache line. A request resulting in the output of both the initial cache line (cache line 1) and prefetch line (cache line 2) would therefore output two cache lines. Hence, the amount of data that can be stored

between two neighboring start address (*i.e.*, one cache line), would be smaller than the amount of data output in response to the request (*i.e.*, two cache lines).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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September 22, 2003

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